





Phase Control Thyristor

Preliminary Information

DS5941-1.0 March 2009 (LN 26624)

FEATURES

- Double Side Cooling
- High Surge Capability

APPLICATIONS

- High Power Drives
- High Voltage Power Supplies
- Static Switches

VOLTAGE RATINGS

Part and Ordering Number	Repetitive Peak Voltages V _{DRM} and V _{RRM} V	Conditions
DCR4330M52* DCR4330M50 DCR4330M45	5200 5000 4500	$\begin{split} &T_{vj} = -40^{\circ}\!\text{C to } 125^{\circ}\!\text{C},\\ &I_{DRM} = I_{RRM} = 300\text{mA},\\ &V_{DRM}, V_{RRM}t_p = 10\text{ms},\\ &V_{DSM}\&V_{RSM} = \\ &V_{DRM}\&V_{RRM} + 100V\\ &respectively \end{split}$

Lower voltage grades available. *5000V @ -40°C, 5200V @ 0°C

ORDERING INFORMATION

When ordering, select the required part number shown in the Voltage Ratings selection table.

For example:

DCR4330M52

Note: Please use the complete part number when ordering and quote this number in any future correspondence relating to your order.

KEY PARAMETERS

V_{DRM}	5200V
I _{T(AV)}	4325A
I _{TSM}	53400A
dV/dt*	2000V/μs
dl/dt	400A/μs

* Higher dV/dt selections available

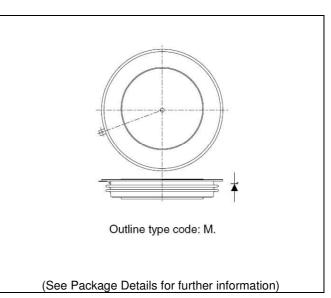


Fig. 1 Package outline





CURRENT RATINGS

T_{case} = 60 °C unless stated otherwise

Symbol	Parameter	Test Conditions	Max.	Units
Double Side Cooled				
I _{T(AV)}	Mean on-state current	Half wave resistive load	4325	Α
I _{T(RMS)}	RMS value	-	6790	Α
I _T	Continuous (direct) on-state current	-	6250	Α

SURGE RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
I _{TSM}	Surge (non-repetitive) on-state current	10ms half sine, T _{case} = 125 ℃	53.4	kA
l ² t	I ² t for fusing	$V_R = 0$	14.25	MA ² s

THERMAL AND MECHANICAL RATINGS

Symbol	Parameter	Test Conditions		Min.	Max.	Units
R _{th(j-c)}	Thermal resistance – junction to case	Double side cooled	DC	-	0.00518	°C/W
		Single side cooled	Anode DC	-	0.01012	°C/W
			Cathode DC	-	0.01080	°C/W
R _{th(c-h)}	Thermal resistance – case to heatsink	Clamping force 83.0kN	Double side	-	0.001	°C/W
		(with mounting compound)	Single side	-	0.002	°C/W
T_{vj}	Virtual junction temperature	On-state (conducting)		-	135	℃
		Reverse (blocking)		-	125	℃
T _{stg}	Storage temperature range			-55	125	℃
Fm	Clamping force			74.0	91.0	kN





DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test Conditions		Min.	Max.	Units
I _{RRM} /I _{DRM}	Peak reverse and off-state current	At V _{RRM} /V _{DRM} , T _{case} = 125 ℃		-	300	mA
dV/dt	Max. linear rate of rise of off-state voltage	To 67% V _{DRM} , T _j = 125℃, ga	ate open	-	2000	V/µs
dl/dt	Rate of rise of on-state current	From 67% V _{DRM} to 2x I _{T(AV)}	Repetitive 50Hz	-	400	A/μs
		Gate source 30V, 10Ω,	Non-repetitive	-	1000	A/μs
		$t_r < 0.5 \mu s, T_j = 125 ^{\circ}C$				
$V_{T(TO)}$	Threshold voltage – Low level	1000 to 2600A at T _{case} = 125	5℃	-	0.85	٧
	Threshold voltage – High level	2600 to 9000A at T _{case} = 125	3°C	-	0.99	٧
r _T	On-state slope resistance – Low level	1000 to 2600A at T _{case} = 125	°℃	-	0.2115	mΩ
	On-state slope resistance – High level	2600 to 9000A at T _{case} = 125 °C		-	0.1578	mΩ
t _{gd}	Delay time	$V_D = 67\% V_{DRM}$, gate source 30V, 10Ω		-	3	μs
		$t_r=0.5\mu s, T_j=25^{\circ}\!\!\mathrm{C}$				
t _q	Turn-off time	T_j = 125 °C, V_R = 200V, dI/dt = 1A/ μ s,			750	μs
		dV _{DR} /dt = 20V/μs linear				
Qs	Stored charge	- I_T = 3000A, T_j = 125 °C, dI/dt – 1A/μs, V_{Rpeak} ~3100V, V_R ~ 2100V		4030	5420	μC
I _{RR}	Reverse recovery current			49	59	А
lι	Latching current	$T_j = 25$ °C, $V_D = 5V$		1	3	А
lн	Holding current	$T_j = 25^{\circ}\text{C}, \; R_{G\text{-K}} = \infty, \; I_{TM} = 500A, \; I_T = 5A$		-	300	mA



GATE TRIGGER CHARACTERISTICS AND RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
V_{GT}	Gate trigger voltage	V _{DRM} = 5V, T _{case} = 25 ℃	1.5	V
V_{GD}	Gate non-trigger voltage	At 50% V _{DRM} , T _{case} = 125 ℃	0.4	V
I _{GT}	Gate trigger current	V _{DRM} = 5V, T _{case} = 25 ℃	300	mA
I _{GD}	Gate non-trigger current	At 50% V _{DRM} , T _{case} = 125 ℃	10	mA

CURVES

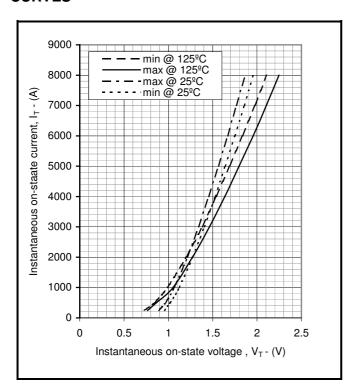


Fig.2 Maximum & minimum on-state characteristics

V_{TM} EQUATION

 $V_{TM} = A + Bln (I_T) + C.I_T + D.\sqrt{I_T}$

Where A = 0.061592

B = 0.115333

C = 0.000119

D = 0.002394

these values are valid for $T_i = 125 \,^{\circ}\text{C}$ for $I_T 250 \,^{\circ}\text{A}$ to 9000A



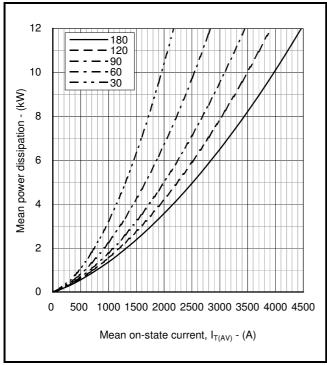


Fig.3 On-state power dissipation - sine wave

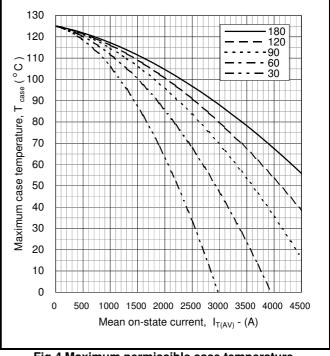


Fig.4 Maximum permissible case temperature, double side cooled – sine wave

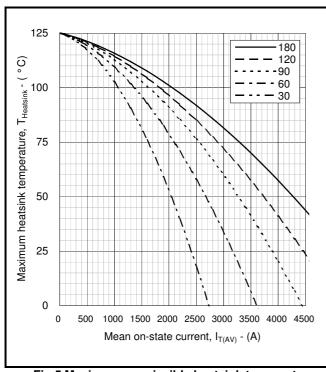


Fig.5 Maximum permissible heatsink temperature, double side cooled – sine wave

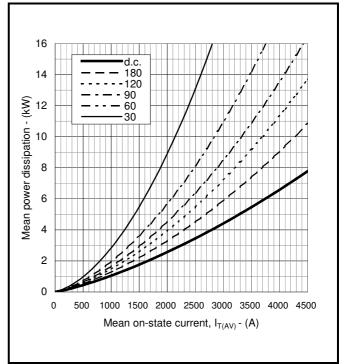


Fig.6 On-state power dissipation - rectangular wave



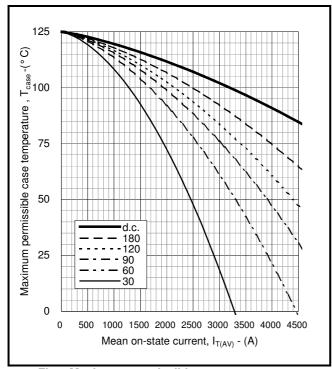


Fig.7 Maximum permissible case temperature, double side cooled – rectangular wave

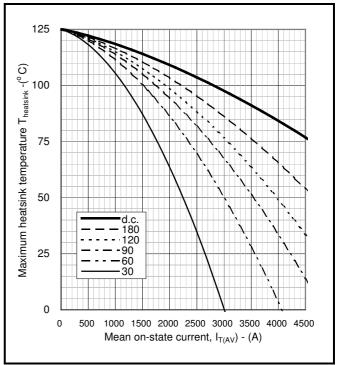
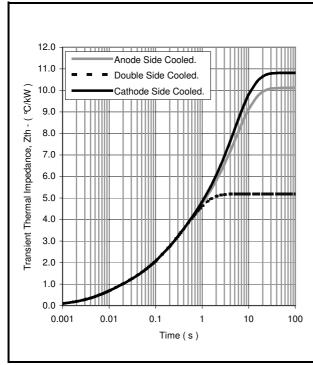


Fig.8 Maximum permissible heatsink temperature, double side cooled – rectangular wave



		1	2	3	4
Double side cooled	R _i (℃/kW)	1.995338	1.242784	1.9448	0.005
Double side cooled	T _i (s)	0.05	0.592935	0.592385	110.5108
Anode side cooled	R _i (℃/kW)	6.092995	1.957372	2.042252	0.035908
Ariode side cooled	T _i (s)	5.459764	0.510898	0.05	110.1735
Cathode side cooled	R _i (℃/kW)	6.856845	1.876401	2.062845	0.025343
Callibde side cooled	T: (s)	5.181139	0.557321	0.05	110.1546

$$Z_{th} = \sum_{i=1}^{i=4} [R_i \times (1 - \exp(T/T_i))]$$

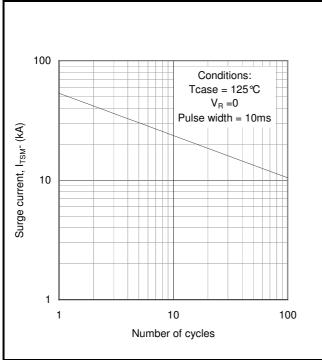
$\Delta R_{th(j\text{-c})}$ Conduction

Table's show the increments of thermal resistance $R_{\text{th}(j\text{-}c)}$ when the device operates at conduction angles other than d.c.

Double side cooling				Anode Side Cooling				
	$\Delta Z_{th}(z)$				ΔZ_t	_h (z)		
θ°	sine.	rect.		θ°	sine.	rect.		
180	0.51	0.36		180	0.51	0.36		
120	0.57	0.49		120	0.58	0.50		
90	0.64	0.56		90	0.65	0.57		
60	0.70	0.63		60	0.71	0.64		
30	0.74 0.71			30	0.75	0.71		

Cat	<u>node Side</u>	d Cooling		
	$\Delta Z_{th}(z)$			
θ°	sine.	rect.		
180	0.51	0.36		
120	0.58	0.50		
90	0.65	0.57		
60	0.71	0.64		
30	0.75	0.71		
15	0.77	0.75		

Fig.9 Maximum (limit) transient thermal impedance – junction to case (°C/kW)





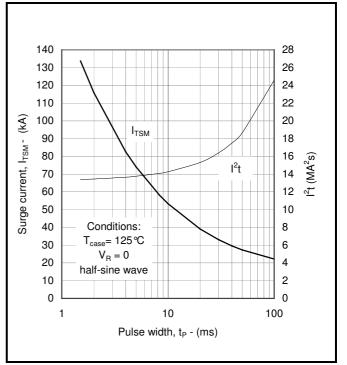


Fig.11 Single-cycle surge current

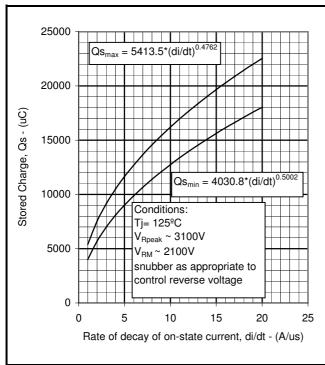


Fig.12 Stored charge

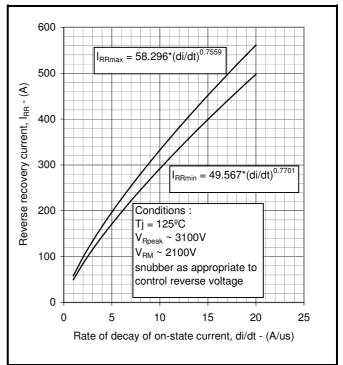


Fig.13 Reverse recovery current

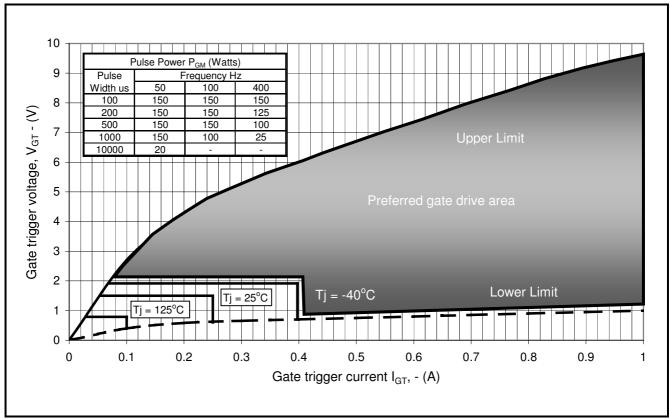


Fig14 Gate Characteristics

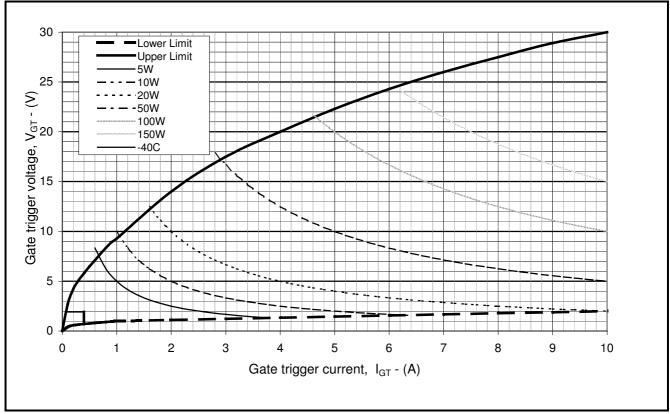


Fig. 15 Gate characteristics





PACKAGE DETAILS

For further package information, please contact Customer Services. All dimensions in mm, unless stated otherwise. DO NOT SCALE.

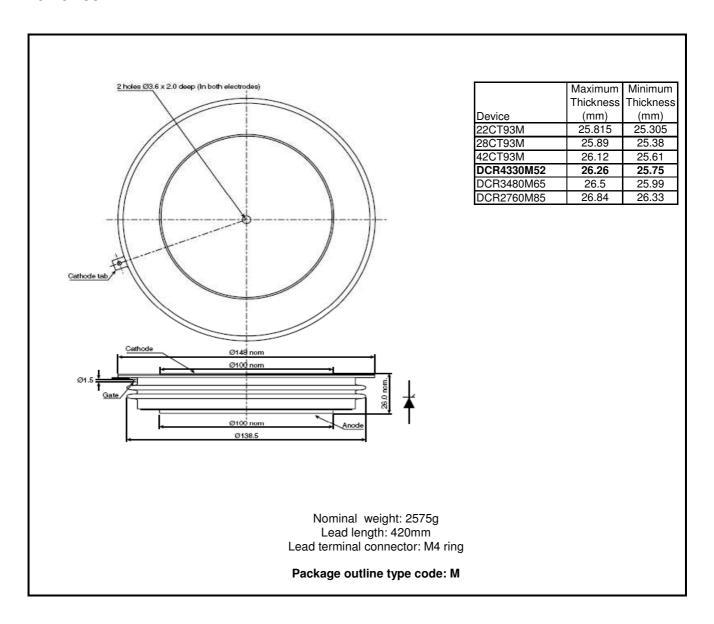


Fig.16 Package outline





POWER ASSEMBLY CAPABILITY

The Power Assembly group was set up to provide a support service for those customers requiring more than the basic semiconductor, and has developed a flexible range of heatsink and clamping systems in line with advances in device voltages and current capability of our semiconductors.

We offer an extensive range of air and liquid cooled assemblies covering the full range of circuit designs in general use today. The Assembly group offers high quality engineering support dedicated to designing new units to satisfy the growing needs of our customers.

Using the latest CAD methods our team of design and applications engineers aim to provide the Power Assembly Complete Solution (PACs).

HEATSINKS

The Power Assembly group has its own proprietary range of extruded aluminium heatsinks which have been designed to optimise the performance of Dynex semiconductors. Data with respect to air natural, forced air and liquid cooling (with flow rates) is available on request.

For further information on device clamps, heatsinks and assemblies, please contact your nearest sales representative or Customer Services.

Stresses above those listed in this data sheet may cause permanent damage to the device. In extreme conditions, as with all semiconductors, this may include potentially hazardous rupture of the package. Appropriate safety precautions should always be followed.



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